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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/822,166	03/30/2001	Ritesh Saraf	03226.082001;P5751	6279

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/822,166	SARAF, RITESH	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,15,17 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,15,17 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

Applicant's arguments filed October 4, 2004 have been fully considered but they are not persuasive.

Applicant argues (page 7 paragraph 3) " The various delayed versions of the clock signal are then used to control the operations of the data input control stage, scan input control stage, master stage and the slave stage. Further, the flip-flop circuit of the present invention utilizes embedded scan logic. Apart from the master stage and the slave stage, no additional latches are used to store the scan input SI which is directly connected to the master stage through a sixth NMOS."

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., 'The various delayed versions of the clock signal are then used to control the operations of the data input control stage, scan input control stage, master stage and the slave stage.' *and* 'Apart from the master stage and the slave stage, no additional latches are used to store the scan input SI which is directly connected to the master stage through a sixth NMOS.') are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to applicant's arguments, the recitation 'the flip-flop circuit of the present invention utilizes embedded scan logic.' has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1-3,5-13, 15, 17-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsunaga et al. U.S. Patent No. 6,150,861.

As per claim 1, Matsunaga et al. teach flip-flop circuitry that includes a data input control stage that selectively controls a value on a data node that is coupled to the master stage and the slave stage and a scan input control stage that selectively controls

a value on a scan node that is coupled to the master stage, and also teaches a data input signal that selectively controls the value on the scan node dependent on the clock input control stage (Fig.2, column 3 lines 30-54). Moreover, Matsunaga et al. teach one of the scan and data nodes being held constant when the other of the scan and data nodes is active (Abstract, claim 9).

As per claim 2, Matsunaga et al. teach flip-flop circuitry wherein the data input control stage inputs a data input signal and a scan enable signal, and wherein the data input control stage resides on the topmost end of the flip-flop circuit (Fig. 1,2).

As per claim 3: Matsunaga et al. teach flip-flop circuitry wherein the scan input control stage inputs a scan input signal and a scan enable signal, wherein the scan input control stage resides on the bottommost end of the flip-flop circuit (Fig. 1,2).

As per claim 5: Matsunaga et al. teach a scan node that is active during the scan mode (Column 2 lines 35- 36).

As per claim 6: Matsunaga et al. teach the scan node being pulled to a second value when the flip-flop is in normal mode, and wherein the data node is active during normal mode (Column 2 lines 33-42).

As per claim 7: Matsunaga et al. teach the master stage passing a value to the slave stage based on the scan and data node values (Fig. 2, Column 3, lines 15-16).

As per claim 8: Matsunaga et al. teach delayed and inverted clock signals to the data and scan input control stages and the master and slave stages (Fig. 1, 2; Column 3 lines 30-45).

As per claim 9: Matsunaga et al. teach a data input signal that selectively controls the value on the data node dependent on the clock input control stage (Column 3 lines 30-54).

As per claim 10, Matsunaga et al. teach a data input signal that selectively controls the value on the scan node dependent on the clock input control stage (Column 3 lines 30-54).

As per claim 11, Matsunaga et al. teach the master stage selectively passing a value to the slave stage dependent on the data and scan nodes and the clock input control stage (Fig.2 Column 3 lines 30-54).

As per claim 12, Matsunaga et al. teach the slave stage selectively controlling the output value of the flip-flop dependent on the data node and the clock input control stage (Fig.2: Column 3 lines 30-54).

As per claim 13, Matsunaga et al. teach flip-flop methodology that includes selectively controlling a value on a data node dependent on a data input control stage and the clock input control stage, wherein the data node is coupled to the master and slave stage, selectively controlling a value on a scan node dependent on a scan input control stage and the clock input control stage, wherein the scan node is coupled to the master stage, selectively controlling the slave stage dependent on the master stage and the clock input control stage, and selectively generating an output of the flip-flop dependent on the slave stage and generating delayed versions of the clock input as it is well known to synchronize the flip-flops (Fig. 1, 2 Column 2 lines 28-67, Column 3 lines

30-54). Moreover, Matsunaga teaches to one of the scan and data nodes being held constant when the other of the scan and data nodes is active (Abstract).

As per claim 15, Matsunaga et al. teach a scan node that is active during the scan mode (Column 2 lines 35-36).

As per claim 17 Matsunaga et al. teach the data node being active during normal mode (Column 2 lines 33-42).

As per claim 18, Matsunaga et al. teach inputting a clock signal to the clock input control stage and generating delayed and inverted clock signals (Fig. 1, 2; Column 3 lines 30-45).

Conclusion

Although the drawings in Figure 5 indicate a different circuit than Matsunaga et al. teach, the claims are not clearly pointing out the differences.

333 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133

Guy J. LAMARRE
PRIMARY EXAMINER